REMARKS

Reconsideration of the above-identified application in view of the foregoing amendments and following remarks is respectfully requested.

A. Claim Status / Explanation of Amendments

Claims 1-6 are pending and were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,316,998 to Oikawa, et al. ("Oikawa") or Japanese Patent Publication No. 04-154312 to Ogawa, et al. ("Ogawa") taken with U.S. Patent Application No. 2002/0011612 to Hieda ("Hieda") and European Patent No. EP 1347506 to Sugawa, et al. ("Sugawa") and further in view of U.S. Patent Application No. 2003/0057439 to Fitzgerald ("Fitzgerald"). [10/22/07 Office Action, p. 2].

By this paper, claims 1 and 6 are amended such that the recitation of "gate widths of a top surface and a side surface of the p-channel MIS field-effect transistor and the n-channel MIS field-effect transistor" is deleted and replaced with the limitation wherein the "height of the side surface of the projecting portion of the p-channel MIS field-effect transistor is set to be different from the height of the side surface of the projecting portion of the n-channel MIS field-effect transistor." Support for the changes to claims 1 and 6 may be found throughout the application as originally filed including, for example, Figs. 3-4 and accompanying descriptive text.

No new matter will be introduced into this application by entry of these amendments. Entry is respectfully requested.

B. Claims 1-6 are Patentably Distinct from the Cited References

Applicants respectfully traverse the 35 U.S.C. § 103(a) rejection of claims 1-6. Oikawa, Ogawa, Hieda, Sugawa, and Fitzgerald, whether taken singly or in combination, do not teach,

disclose or suggest each and every element of these claims. In particular, the cited references fail to disclose differing side surface heights for the projecting portion of the n- and p-channel MIS field effect transistors (MISFET). Accordingly, a rejection for obviousness is improper.

Applicants' claim 1, as amended, recites:

> A DC amplifier formed on a substrate of a semiconductor integrated circuit, comprising
>
> a differential amplification circuit including a p-channel MIS field-effect transistor and an n-channel MIS field-effect transistor in which a projecting portion is formed by a silicon substrate having a first crystal surface as a primary surface and a second crystal surface as a side surface, terminated hydrogen on the silicon surface is removed in plasma atmosphere of an inert gas, then a gate insulating film is formed on at least a part of a top surface and the side surface of the projecting portion at a temperature at or lower than about 550°C in the plasma atmosphere, a gate is formed on the gate insulating film, and a drain and a source are formed on both sides enclosing the gate insulating film of the projecting portion, wherein
>
> the height of the side surface of the projecting portion of the p-channel MIS field-effect transistor is set to be different from the height of the side surface of the projecting portion of the n-channel MIS field-effect transistor, and the current drive capability of the p-channel MIS field-effect transistor can be substantially equal to current drive capability of the n-channel MIS field-effect transistor.

At the outset, the Office Action contends that both Oikawa and Ogawa disclose a DC amplifier comprising a "differential amplification circuit including a MISFET transistor" as recited in Applicants' pending claim 1. However, as recognized and asserted by the Office Action, neither Oikawa or Ogawa teach a MISFET comprised of a three-dimensional structure having a "first crystal surface as a primary surface" and a "second crystal surface as a side surface" wherein the "current drive capability of the p-channel MIS field-effect transistor can be substantially equal to ... the n-channel." [10/22/07 Office Action, p. 2 and 4].

In attempting to remedy these deficiencies, the Office Action relies on Hieda and Fitzgerald, contending that Hieda discloses a MISFET comprising a projection portion formed by a silicon substrate having a first and second crystal surface which serve as primary and side surfaces, respectively, [10/22/07 Office Action, p. 2] and that Fitzgerald discloses that n-channel and p-channel transistors can be designed to provide an approximately equal driving capability by adjusting the gate width [10/22/07 Office Action, p. 4]. The Office Action then contends it would have been obvious to employ the MIS transistors of Heida and modified gate widths as taught by Fitzgerald in the DC amplifier circuits disclosed by Oikawa and Ogawa.

Applicants respectfully disagree and note that if the gate width in conventional MOS transistors having a planar structure is designed such that the current drive capability of the p-channel MOS transistor is equal to that of the n-channel it will be difficult to integrate the devices into a standard semiconductor integrated circuit (IC) since the size of the p-channel MOS transistor will be enlarged and, as such, will require repositioning of adjacent circuitry. Consequently, adjusting the gate width of individual devices constituting a standard IC in order to make the current drive capability equal is not a viable option. Furthermore, desired changes in device performance are traditionally obtained by adjusting the dimensions (i.e., the gate width and length) within the two-dimensional plane of the surface. As such, Applicants respectfully assert that there is provided absolutely no teaching, suggestion, or motivation for accomplishing this by projecting the gate vertically, into a third dimension.

Applicants further note that none of the cited references disclose using differing "projection portion" heights in order to obtain the different gate widths necessary to equate the current drive capabilities of the n- and p-channel MIS transistors. That is, the cited references fail to disclose that the "height of the side surface of the projecting portion of the p-channel MIS

field-effect transistor is set to be different from the height of the side surface of the projecting portion of the n-channel MIS field-effect transistor" as recited in Applicants' amended claim 1. In Heida, for example, only a single height for the 'fence' (13) is illustrated in each of the drawings provided. By utilizing Applicants' three-dimensional structure with differing projection portion heights it is possible to incorporate MOS transistors with larger gate widths without increasing the required area within the two-dimensional plane of the substrate surface.

Accordingly, Oikawa, Ogawa, Hieda, Sugawa, and Fitzgerald - whether alone or in combination - fail to teach, disclose or suggest a DC amplifier formed on a substrate of a semiconductor integrated circuit wherein a "height of the side surface of the projecting portion of the p-channel MIS field-effect transistor is set to be different from the height of the side surface of the projecting portion of the n-channel MIS field-effect transistor" and wherein the "current drive capability of the p-channel MIS field-effect transistor can be substantially equal to the current drive capability of the n-channel MIS field-effect transistor" as recited in Applicants' amended claim 1. Applicants respectfully submit that claim 1 is patentably distinct from Mitsuru, Oikawa, Ogawa, Hieda, Sugawa, and Fitzgerald for at least this reason. Claim 6 is directed to a semiconductor integrated circuit comprising the DC amplifier of claim 1 and, as such, is asserted to be patentably distinct for at least similar reasons. Claims 2-5 depend either directly or indirectly from claim 1 and are asserted to be in condition for allowance for at least similar reasons. The Section 103 rejection should therefore be withdrawn. Applicants respectfully submit that all of the pending claims are now allowable for the above reasons and early, favorable action in that regard is requested.

Applicants have chosen in the interest of expediting prosecution of this patent application to distinguish the cited documents from the pending claims as set forth above. These statements

should not be regarded in any way as admissions that the cited documents are, in fact, prior art. Finally, Applicants have not specifically addressed the rejections of the dependent claims. Applicants respectfully submit that the independent claim, from which they depend, is in condition for allowance as set forth above. Accordingly, the dependent claims are also in condition for allowance. Applicants, however, reserve the right to address such rejections of the dependent claims in the future as appropriate.

CONCLUSION

For the above-stated reasons, this application is respectfully asserted to be in condition for allowance. An early and favorable examination on the merits is earnestly solicited. In the event that a telephone conference would facilitate the examination of this application in any way, the Examiner is invited to contact the undersigned at the number provided.

THE COMMISSIONER IS HEREBY AUTHORIZED TO CHARGE ANY ADDITIONAL FEES WHICH MAY BE REQUIRED FOR THE TIMELY CONSIDERATION OF THIS AMENDMENT UNDER 37 C.F.R. §§ 1.16 AND 1.17, OR CREDIT ANY OVERPAYMENT TO DEPOSIT ACCOUNT NO. 13-4500, ORDER NO. 5000-5296.

Respectfully submitted,
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Dated: January 10, 2008

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